FUJITSU

NMOS UNIVERSAL PERIPHERAL INTERFACE 8-BIT MICROCOMPUTER

MBL8742H/N

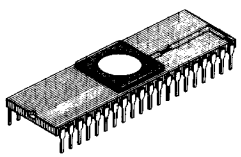
October 1986
Edition 1.0

DESCRIPTION

The Fujitsu MBL8742 Universal Peripheral Interface (UPI) is an 8-bit microcomputer that uses a 2K × 8-bit Electrically Programmable Read Only Memory (EPROM). Besides the EPROM program memory, the microprocessing circuits are supported by a 256 × 8-bit static RAM, 18 I/O lines, an 8-bit timer counter, and a clock generator. The device can be ordered in either of two speed versions: N-version for operation at 6MHz and H-version for operation at 12MHz. For either frequency, the operating temperature is 0°C to 70°C.

The MBL8742 is fabricated using an N-channel polysilicon-gate MOS process and is housed in a 40-pin ceramic windowed DIP. A single +5-volt supply is required for basic operation; the EPROM requires an ultraviolet (UV) light source for erasure and a 21-volt supply for programming.

Using the EPROM program memory, the MBL8742 is ideally suited for such applications as system evaluation, system prototyping, and low-volume production work.

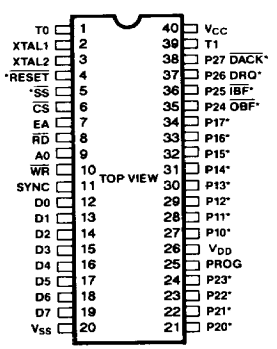


Ceramic DIP
(DIP-40C-A04)

FEATURES

- Processor: 8-bit Microprocessing Unit (MPU)
- Memories: 2K × 8-bit Program Memory (EPROM)
  256 × 8-bit Data Memory (static RAM)
  — 8-level Stack
  — 8 pairs of Working Registers
- I/O: One 8-bit Bidirectional Data Bus
  Two 8-bit Bidirectional I/O Ports
  Two Test Inputs
- Master Processor Interface: One 8-bit Status Register
  Two 8-bit Data Bus Buffer Registers
- DMA Handshake Capability
- 8-bit Timer/Event Counter
- Clock Source: Internal Clock Generator (with external Crystal) or External Clock
- Single-step Operation
- Low-power RAM Retention Mode
- Power-on Reset Capability (with External Capacitor)
- Instruction Cycle: 1.25μs/12MHz (MBL8742H) and 2.5μs/6MHz (MBL8742N)
- Instruction Set: 93 Instructions with 217 Instruction Codes
- Single +5V Power Supply
- Operating Temperature Range: 0°C to 70°C

Pin Assignment



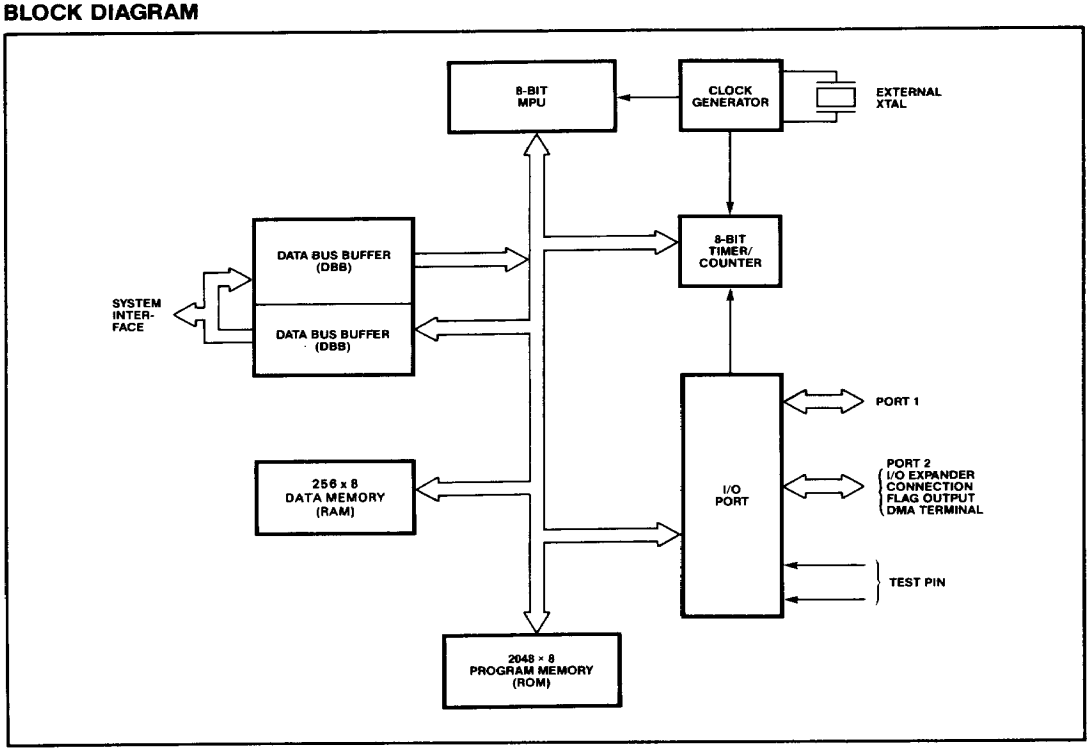
*These pins are internally pulled up.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES (Cont)

- N-channel Silicon-gate MOS Process
- Standard 40-pin Ceramic DIP (Suffix—C)
- Compatible with Intel 8742
- Replaceable with MBL8041A/42 and Intel 8041A/42

BLOCK DIAGRAM



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PIN DESCRIPTIONS

Pin No.	Symbol	Function
40	V_{CC}	+5Vdc power supply input.
26	V_{DD}	+5Vdc power supply input for internal RAM. This pin is also used as the power supply input when programming the EPROM.
20	V_{SS}	Ground terminal.
1	T0	Input used for conditional branching.
39	T1	This pin performs the following functions: • Event input pin for the event counter. • Conditional input pin for conditional branch.

PIN DESCRIPTIONS (Cont)

Pin No.	Symbol	Function
2	XTAL 1	Input connection for external crystal. This pin can also be used as an input from an external clock source.
3	XTAL 2	Input connection for external crystal. (Note: The XTAL 1 and XTAL 2 input levels are not directly TTL compatible with a TTL clock source. An open-collector drive with an appropriate pullup is required to properly interface the two circuits.)
4	$\overline{\text{RESET}}$	Input that resets and initializes the MPU. (Note: This input level is not TTL compatible.)
5	$\overline{\text{SS}}$	Input used for single step operation.
6	$\overline{\text{CS}}$	Chip select input.
7	EA	Input used for controlling program memory access. Holding EA high forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification.
8	$\overline{\text{RD}}$	Strobe that enables a read operation from data bus buffer or status register.
9	A0	Address input to determine whether read/write data or read/write commands. A0 = "L" indicates data read or write. A0 = "H" indicates status read or command write.
10	$\overline{\text{WR}}$	Strobe that enables a write operation to data bus buffer register.
11	SYNC	An output synchronized with the MBL8742 clock. This pin is used when a synchronization signal is required for external circuits.
12-19	D0-D7	8-bit bidirectional I/O port used to interface the MBL8742 to the master processor.
21-24	P20-P23	Lower 4 bits of the 8-bit quasi-bidirectional I/O port (Port 2). These pins function as an interface port with the I/O expander (MBL8243) when an expansion I/O is used to execute instructions. During single step operation the upper 3 bits of the program address are output on P20, P21, P22.
35-38	P24-P27	Upper 4 bits of the 8-bit quasi-bidirectional I/O port (Port 2). These function as the flag output pins (P24 and P25) and DMA pins (P26 and P27) according to the executed instruction. P24: OBF (Output Data Buffer Register Full) output P25: $\overline{\text{IBF}}$ (Input Data Buffer Register Full) output P26: DRQ (DMA Request) output P27: $\overline{\text{DACK}}$ (DMA Acknowledge) input
25	PROG	Strobe output signal when performing an expansion I/O instruction with an I/O expander such as the MBL8243. Used as a programming input when writing to the EPROM.
27-34	P10-P17	8-bit Quasi-bidirectional I/O ports (Port 1). During single step operation, the next program fetch address (Lower 8 bits) is output from these pins.

FUNCTIONAL DESCRIPTION

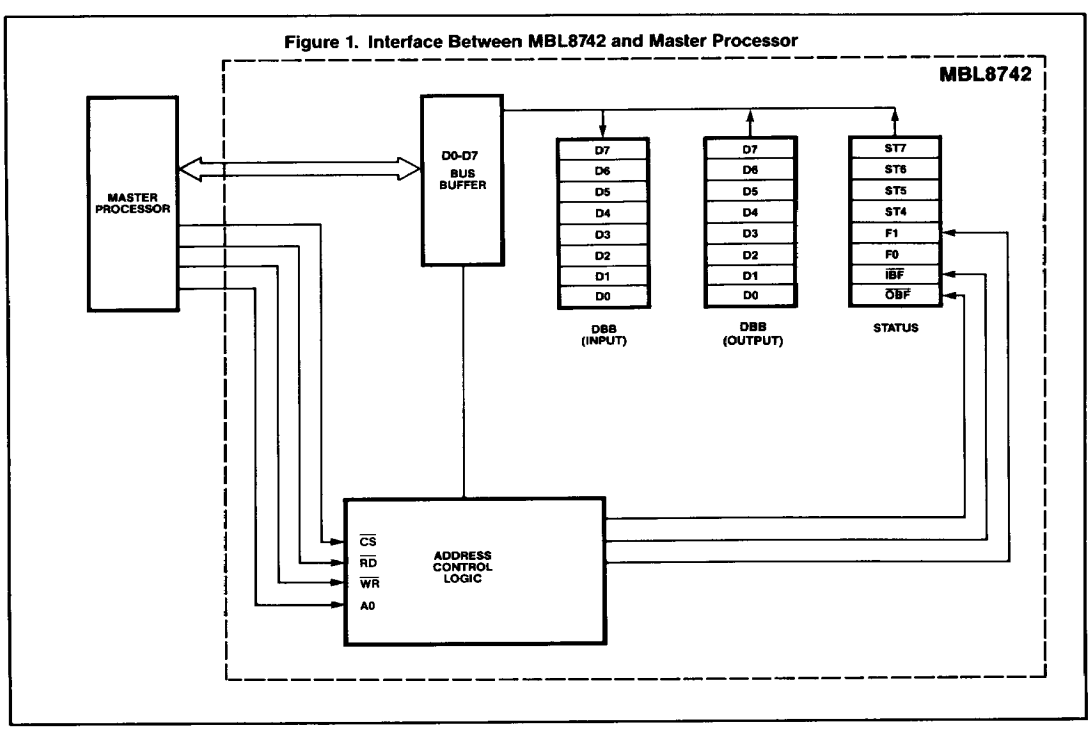
System Interface

The data, command, and status interface between the master processor and the MBL8742 is provided by two Data Bus Buffer(DBB) registers and a status register. Selection logic for these registers is shown in Table 1; a simplified interface is shown in Figure 1. Referring to the interface drawing, note that the master processor can read data from the output buffer register and write data into the input buffer register. When the MBL8742 executes an "OUT DBB, A" instruction, data is written into the DBB and the Output Buffer Full (OBF) flag is set. When data is read from the DBB by the master processor, OBF is reset. If the master processor writes into DBB, the Input Buffer Full ($\overline{IBF}$) flag is set and is reset when the MBDL8742 reads the data. Reading the status register is non-destructive and does not affect internal operation of the MBL8742.

Table 1. Selection Logic

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	AO	DESCRIPTION
0	0	1	0	Read DBB (Output) register.
0	0	1	1	Read STS (Output) register (Status)
0	1	0	0	Write DBB (Input) register (Data).
0	1	0	1	Write DBB (Input) register (Command).
1	x	x	x	Invalid.

Figure 1. Interface Between MBL8742 and Master Processor



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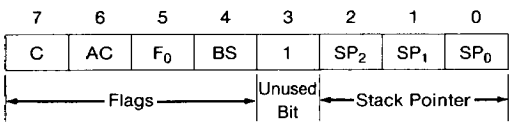
Program Status Word (PSW)

As shown in the following diagram and associated text, the upper four bits of the PSW are used as flags to indicate MPU status. The lower three bits are used to select register pairs in the RAM stack when servicing a subroutine call or an interrupt. The flag bits (C, AC, F_0, and BS) are defined below; the stack pointer bits (SP_0 - SP_2) are defined in the next paragraph. The remaining bit in the PSW is unused.



Flag Bits

C (Carry): When an accumulator overflow occurs during an ALU operation, this bit is set to '1'.

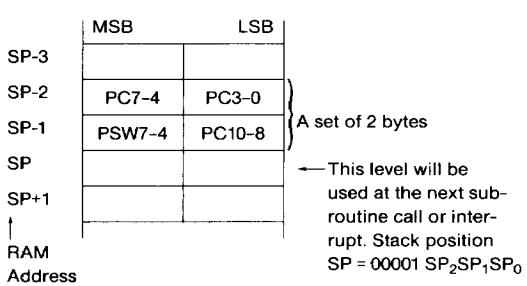
AC (Auxiliary Carry): When an accumulator overflow from bit 3 to bit 4 occurs during an addition, this bit is set to "1".

F_0 (User Flag): With the proper instruction, this flag can be user-designated; the F_0 flag can also be checked from the MPU as bit 2 of the Status Register.

BS (Bank Select): With the proper instruction, the BS flag indicates selection of a Register Bank. When set to "0", Register Bank 0 is selected; when set to "1", Register Bank 1 is selected. Refer to the RAM memory map that follows.

Stack Register (8-Level Capability)

The Stack Register has 16 bytes of memory area in the built-in RAM. The stack Register consists of eight levels, that is, a stack level consists of two bytes as shown in the following diagram.

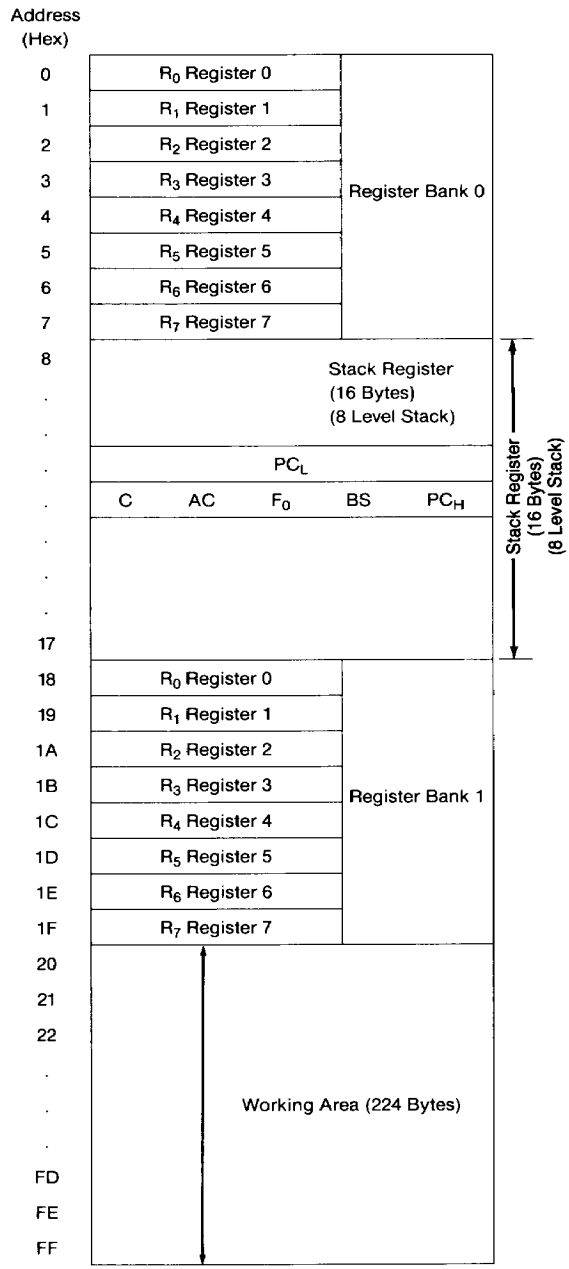


SP (Stack Pointer): In the above figure, "SP" indicates an address of Stack Pointer to be used for the next sub-routine call or interrupt. "SP" is given as an 8-bit code from the lower three bits of Status Register as follows:

SP = 00001$SP_2SP_1SP_0$ → Status Register Bits 0 to 2.

PC_n (Program Counter): In the above figure, "PC_n" indicates the content of the n-th bit in the Program Counter.

RESIDENT DATA MEMORY MAP (RAM)



Interrupt Processing

There are two types of interrupt: $\overline{IBF}$ interrupt and Timer/Counter interrupt. If an interrupt occurs when the system is in "interrupt enable" status, the interrupt flag is set as soon as the current instruction is completed and interrupt processing starts.

First, the upper four bits of the Status Word and content of the Program Counter are stored in the stack. The program then jumps to address "3" in the case of an $\overline{IBF}$ interrupt and address "7" in the case of a Timer/Counter interrupt.

After the interrupt has been processed by a user program and a RETR (Return and Restore Status) instruction has been executed, the Status Word and Program Counter contents stored in the stack are restored, the interrupt flag is reset, and the system is ready to accept the next interrupt request.

A Timer/Counter interrupt request occurs when the Timer/Counter overflow flag is set due to Timer/Counter overflow. However, since the Timer/Counter interrupt request is masked by the $\overline{IBF}$ interrupt request, an $\overline{IBF}$ interrupt has first priority.

The Timer/Counter interrupt is enabled after the $\overline{IBF}$ interrupt has been executed and the system is now ready to receive the next interrupt request. Operational and interrupt flowcharts are shown on the following page.

PROGRAMMING AND VERIFYING THE EPROM

The MBL8742 uses an internal 2K × 8 EPROM for program memory. A description of the pins used for programming and verifying operation of the EPROM are repeated here for user convenience. Procedural steps for programming and verification follow the pin functions.

Pin Descriptions

Symbol	Function
XTAL1 & XTAL2	Input clock signal (1-to-3MHz)
$\overline{RESET}$	Initializes internal registers. Input address data to the data bus is internally latched on the rising edge of $\overline{RESET}$.
T0	When T0 is Low, program mode is selected. When T0 is High, verify mode is selected.
EA	When 18-volts is applied to this pin, the program and verify modes are enabled.
Bus (D7-D0)	Lower 8-bits for address and data inputs in the program mode; data output in the verify mode.
P22-P20	Upper address inputs.
V_{DD}	+5-volt power supply.
PROG	Input programming pulses.
A0 & $\overline{CS}$	Clamp both of these inputs low.

Programming Procedures

Step 1: Initialize circuits as follows.

- Apply +5V to V_{CC}, V_{DD}, T0 and EA pins. Let Bus (D7-D0) and PROG pins float.
- Apply 0V to $\overline{RESET}$, A0, and $\overline{CS}$ pins.
- Use internal oscillator or an external source to generate a 1-to-3MHz clock.

Step 2: Select program mode by setting T0 to 0V.

Step 3: Set EA to 18V to enable program or verify mode.

Step 4: Input address as follows.

- Bus (D7-D0): 8 low-order bits
- P22 to P20: 3 high-order bits

Step 5: Set $\overline{RESET}$ to +5V to internally latch address inputs.

Step 6: Input write data to bus.

Step 7: Turn on programming power supply and set V_{DD} to 21-volts.

Step 8: Apply 0-volts to the PROG pin and then apply a programming pulse of 18-volts for 50-milliseconds. Again apply 0-volts to the pin and then let it float.

Step 9: Turn off programming power supply (V_{DD} from 21V to 5V) and let Bus (D7-D0) float.

Step 10: Select verify mode by setting T0 to 5V.

Step 11: Read and verify bus data. If data cannot be verified, repeat steps 2 through 10.

Step 12: Set $\overline{RESET}$ to 0V. If all desired addresses haven't been written yet, repeat steps 4 through 11.

Step 13: Set EA to 5V to terminate programming procedure.

ERASING THE EPROM

Data written into the EPROM can be erased by applying ultraviolet light rays with a wavelength of 2537 angstroms. With UV light source directly above the transparent lid at a distance of 2-to-3 centimeters. The time for complete erasure is between 15-and-20 minutes for most commercial lamps. The recommended amount of UV radiation is 10Wsec/cm^2; the luminous intensity on the package surface is designed to be approximately 12000uW/cm^2.

If the package surface is soiled by grease, adhesives, or other light inhibitors, the erasing time will increase. Before attempting to erase data, it is recommended that surfaces be cleaned with alcohol or some other detergent that will not damage the package.

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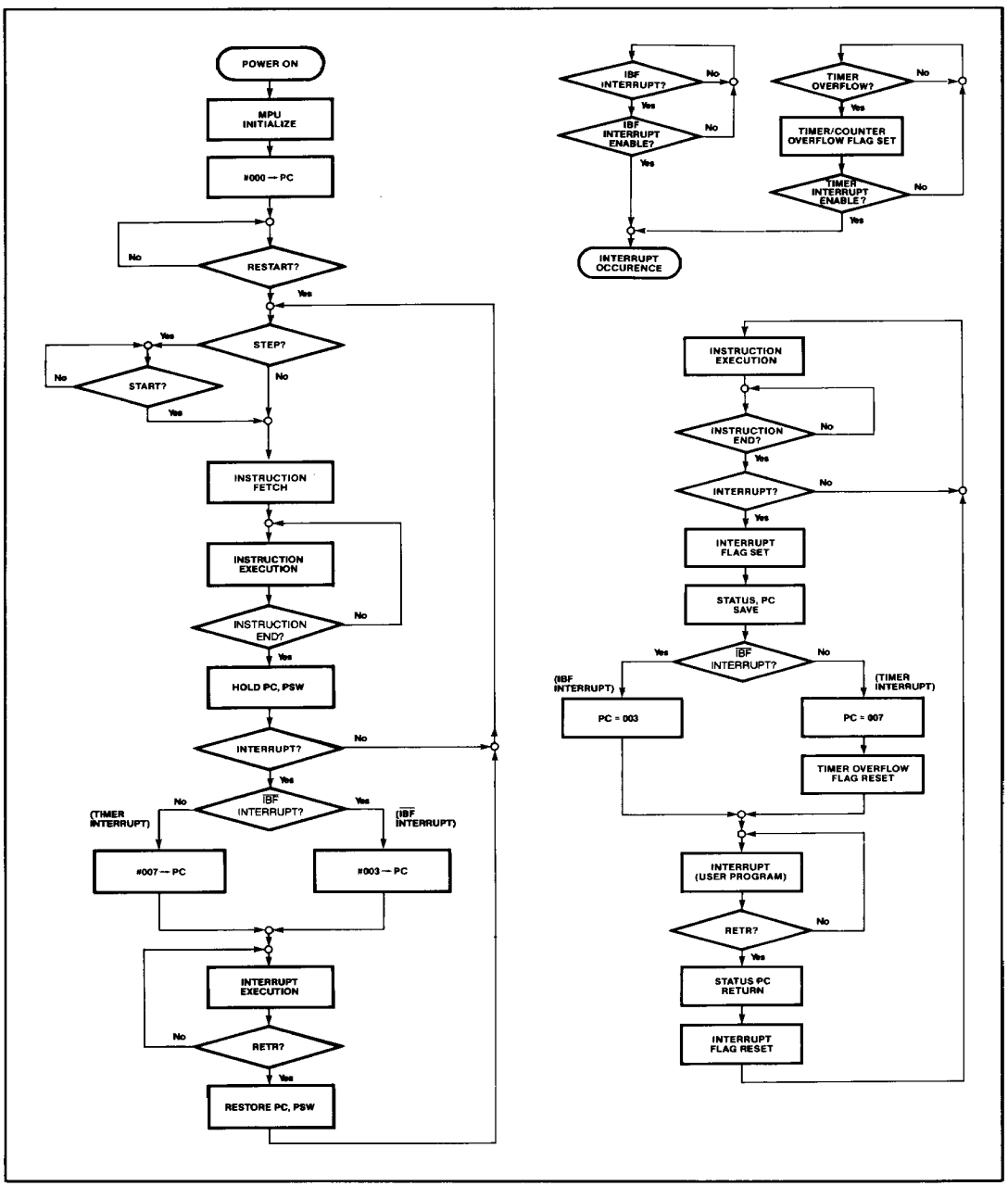
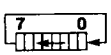
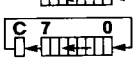
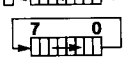
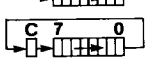
OPERATIONAL FLOWCHART



INTERRUPT FLOWCHART

Table 2. Instruction Set Summary

Operation	Mnemonic	OP code	Byte	Cycle	Flag C	Flag AC	Remarks
ACCUMULATOR INSTRUCTIONS							
Add register to A	ADD A, Rr	6X[3]	1	1	*[2]	*[2]	(A) ← (A) + (Rr)
Add data memory to A	ADD A, @R0	60	1	1	*[2]	*[2]	(A) ← (A) + ((R0))
	ADD A, @R1	61	1	1	*[2]	*[2]	(A) ← (A) + ((R1))
Add immediate to A	ADD A, #data	03	2	2	*[1]	*[2]	(A) ← (A) + data
Add register to A with Carry	ADDC A, Rr	7X[3]	1	1	*[1]	*[2]	(A) ← (A) + (Rr) + (C)
Add data memory to A with Carry	ADDC A, @R0	70	1	1	*[1]	*[2]	(A) ← (A) + ((R0)) + (C)
	ADDC A, @R1	71	1	1	*[1]	*[2]	(A) ← (A) + ((R1)) + (C)
Add immediate to A with Carry	ADDC A, #data	13	2	2	*[1]	*[2]	(A) ← (A) + data + (C)
AND register to A	ANL A, Rr	5X[3]	1	1	-	-	(A) ← (A) AND (Rr)
AND data memory to A	ANL A, @R0	50	1	1	-	-	(A) ← (A) AND ((R0))
	ANL A, @R1	51	1	1	-	-	(A) ← (A) AND ((R1))
AND immediate to A	ANL A, #data	53	2	2	-	-	(A) ← (A) AND data
OR register to A	ORL A, Rr	4X[3]	1	1	-	-	(A) ← (A) OR (Rr)
OR data memory to A	ORL A, @R0	40	1	1	-	-	(A) ← (A) OR ((R0))
	ORL A, @R1	41	1	1	-	-	(A) ← (A) OR ((R1))
OR immediate to A	ORL A, #data	43	2	2	-	-	(A) ← (A) OR data
Exclusive OR register to A	XRL A, Rr	DX[3]	1	1	-	-	(A) ← (A) XOR (Rr)
Exclusive OR data memory to A	XRL A, @R0	D0	1	1	-	-	(A) ← (A) XOR ((R0))
	XRL A, @R1	D1	1	1	-	-	(A) ← (A) XOR ((R1))
Exclusive OR immediate to A	XRL A, #data	D3	2	2	-	-	(A) ← (A) XOR data
Increment A	INC A	17	1	1	-	-	(A) ← (A) + 1
Decrement A	DEC A	07	1	1	-	-	(A) ← (A) - 1
Clear A	CLR A	27	1	1	-	-	(A) ← 0
Complement A	CPL A	37	1	1	-	-	(A) ← ($\bar{A}$)
Decimal Adjust A	DA A	57	1	1	*	-	Note 2
Swap digits of A	SWAP A	47	1	1	-	-	(A7-4) ⇄ (A3-0)
Rotate A Left	RL A	E7	1	1	-	-	
Rotate A Left through Carry	RLC A	F7	1	1	*[1]	-	
Rotate A Right	RR A	77	1	1	-	-	
Rotate A Right through Carry	RRC A	67	1	1	*[1]	-	
INPUT/OUTPUT INSTRUCTIONS							
Input port to A	IN A, P1	09	1	2	-	-	(A) ← (P1)
	IN A, P2	0A	1	2	-	-	(A) ← (P2)
Output A to port	OUTL P1, A	39	1	2	-	-	(P1) ← (A)
	OUTL P2, A	3A	1	2	-	-	(P2) ← (A)
AND immediate to port	ANL P1, #data	99	2	2	-	-	(P1) ← (P1) AND data
	ANL P2, #data	9A	2	2	-	-	(P2) ← (P2) AND data
OR immediate to port	ORL P1, #data	89	2	2	-	-	(P1) ← (P1) OR data
	ORL P2, #data	8A	2	2	-	-	(P2) ← (P2) OR data
Input DBB to A, clear IBF	IN A, DBB	22	1	1	-	-	(A) ← (DBB), (IBF) ← 0
Output A to DBB, set OBF	OUT DBB, A	02	1	1	-	-	(DBB) ← (A), (OBF) ← 1
A7-4 to bits 7-4 of Status	MOV STS, A	90	1	1	-	-	(STS7-4) ← (A7-A4)

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INPUT/OUTPUT INSTRUCTIONS (Continued)

Operation	Mnemonic	OP code	Byte	Cycle	Flag C	Flag AC	Remarks
Input Expander port to A	MOVD A, Pp	OX^4	1	2	-	-	(A3-0) ← (Pp), (A7-4) ← 0
Output A to Expander port	MOVD Pp, A	$3X^4$	1	2	-	-	(Pp) ← (A3-0)
AND A to Expander port	ANLD Pp, A	$9X^4$	1	2	-	-	(Pp) ← (Pp) AND (A3-0)
OR A to Expander port	ORLD Pp, A	$8X^4$	1	2	-	-	(Pp) ← (Pp) OR (A3-0)
DATA MOVE INSTRUCTIONS							
Move register to A	MOV A, Rr	FX^3	1	1	-	-	(A) ← (Rr)
Move data memory to A	MOV A, @R0	F0	1	1	-	-	(A) ← ((R0))
	MOV A, @R1	F1	1	1	-	-	(A) ← ((R1))
Move immediate to A	MOV A, #data	23	2	2	-	-	(A) ← data
Move A to register	MOV Rr, A	AX^3	1	1	-	-	(Rr) ← (A)
Move A to data memory	MOV @R0, A	A0	1	1	-	-	((R0)) ← (A)
	MOV @R1, A	A1	1	1	-	-	((R1)) ← (A)
Move immediate to register	MOV Rr, #data	BX^3	2	2	-	-	(Rr) ← data
Move immediate to data memory	MOV @R0, #data	B0	2	2	-	-	((R0)) ← data
	MOV @R1, #data	B1	2	2	-	-	((R1)) ← data
Move PSW to A	MOV A, PSW	C7	1	1	-	-	(A) ← (PSW)
Move A to PSW	MOV PSW, A	D7	1	1	*1	*1	(PSW) ← (A)
Exchange A and register	XCH A, Rr	$2X^3$	1	1	-	-	(A) ⇄ (Rr)
Exchange A and data memory	XCH A, @R0	20	1	1	-	-	(A) ⇄ ((R0))
	XCH A, @R1	21	1	1	-	-	(A) ⇄ ((R1))
Exchange digit of A and data memory	XCHD A, @R0	30	1	1	-	-	(A3-0) ⇄ ((R0)3-0)
	XCHD A, @R1	31	1	1	-	-	(A3-0) ⇄ ((R1)3-0)
Move to A from current page	MOVP A, @A	A3	1	2	-	-	(A) ← ((A)) within page
Move to A from Page 3	MOVP3A, @A	E3	1	2	-	-	(A) ← ((A)) within page 3
TIMER/COUNTER INSTRUCTIONS							
Read Timer/Counter	MOV A, T	42	1	1	-	-	(A) ← (T)
Load Timer/Counter	MOV T, A	62	1	1	-	-	(T) ← (A)
Start Timer	STRT T	55	1	1	-	-	
Start Counter	STRT CNT	45	1	1	-	-	
Stop Timer/Counter	STOP TCNT	65	1	1	-	-	
Enable Timer/Counter Interrupt	EN TCNTI	25	1	1	-	-	
Disable Timer/Counter Interrupt	DIS TCNTI	35	1	1	-	-	
CONTROL INSTRUCTIONS							
Enable DMA Handshake Lines	EN DMA	E5	1	1	-	-	
Enable IBF Interrupt	EN I	05	1	1	-	-	
Disable IBF Interrupt	DIS I	15	1	1	-	-	
Enable Master Interrupts	EN FLAGS	F5	1	1	-	-	
Select register bank 0	SEL RB0	C5	1	1	-	-	(BS) ← 0
Select register bank 1	SEL RB1	D5	1	1	-	-	(BS) ← 1
No Operation	NOP	00	1	1	-	-	
REGISTER INSTRUCTIONS							
Increment register	INC Rr	$1X^3$	1	1	-	-	(Rr) ← (Rr) + 1
Increment data memory	INC @R0	10	1	1	-	-	((R0)) ← ((R0)) + 1
	INC @R1	11	1	1	-	-	((R1)) ← ((R1)) + 1
Decrement register	DEC Rr	CX^3	1	1	-	-	(Rr) ← (Rr) - 1

Operation	Mnemonic	OP code	Byte	Cycle	Flag C	Flag AC	Remarks
SUBROUTINE INSTRUCTIONS							
Jump to Subroutine	CALL addr	%4[5]	2	2	-	-	Note 6
Return	RET	83	1	2	-	-	Note 7
Return and restore status	RETR	93	1	2	*[1]	*[1]	Note 8
FLAGS INSTRUCTIONS							
Clear Carry	CLR C	97	1	1	Z[1]	-	(C) ← 0
Complement Carry	CPL C	A7	1	1	CP[1]	-	(C) ← $(\overline{C})$
Clear Flag 0	CLR F0	85	1	1	-	-	(F0) ← 0
Complement Flag 0	CPL F0	95	1	1	-	-	(F0) ← $(\overline{F0})$
Clear Flag 1	CLR F1	A5	1	1	-	-	(F1) ← 0
Complement Flag 1	CPL F1	B5	1	1	-	-	(F1) ← $(\overline{F1})$
BRANCH INSTRUCTIONS							
Jump unconditional	JMP addr	%4[5]	2	2	-	-	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	-	-	Unconditional Branch (Note 9)
Decrement register and jump	DJNZ Rr, addr	EX[3]	2	2	-	-	(Rr) ≠ 0 (Note 10)
Jump on Carry = 1	JC addr	F6	2	2	-	-	(C) = 1
Jump on Carry = 0	JNC addr	E6	2	2	-	-	(C) = 0
Jump on A Zero	JZ addr	C6	2	2	-	-	(A) = 0
Jump on A not Zero	JNZ addr	96	2	2	-	-	(A) ≠ 0
Jump on T0 = 1	JT0 addr	36	2	2	-	-	(T0) = H
Jump on T0 = 0	JNT0 addr	26	2	2	-	-	(T0) = L
Jump on T1 = 1	JT1 addr	56	2	2	-	-	(T1) = H
Jump on T1 = 0	JNT1 addr	46	2	2	-	-	(T1) = L
Jump on F0 = 1	JF0 addr	B6	2	2	-	-	(F0) = 1
Jump on F1 = 1	JF1 addr	76	2	2	-	-	(F1) = 1
Jump on Timer Flag = 1, Clear Flag	JTF addr	16	2	2	-	-	(TF) = 1
Jump on IBF Flag = 0	JNIBF addr	D6	2	2	-	-	(IBF) = 0
Jump on OBF Flag = 1	JOBF addr	86	2	2	-	-	(OBF) = 1
Jump on Accumulator Bit	JBb addr	%2[5]	2	2	-	-	(Ab) = 1

Notes:

1. Flag status
   * = Set or reset flag bit to the state it was in before instruction execution.
   Z = Reset flag bit.
   CP = Complement flag bit.
2. The accumulator value is adjusted to form BCD digits following the binary addition of BCD numbers.
3. Refer to Table 3.
4. Refer to Table 4.
5. Refer to Table 5.
6. CALL addr
   ((SP)) ← (PC), (PSW7-4)
   (SP) ← (SP) + 1
   $(PC10\text{-}8) \leftarrow A_H$
   $(PC7\text{-}0) \leftarrow A_L$
7. RET
   (SP) ← (SP) - 1
   (PC) ← ((SP))
8. RETR
   (SP) ← (SP) - 1
   (PC) ← ((SP))
   (PSW7-4) ← ((SP))
9. JMPP @A
   (PC7-0) ← ((A))
10. DJNZ Rr, addr
    (Rr) ← (Rr) - 1
    if (Rr) ≠ 0 (PC7-0) ← addr
    if (Rr) = 0 Execute next instruction

4

Table 3. OP Code for Register Access

Mnemonic / Rr	R0	R1	R2	R3	R4	R5	R6	R7
ADD A, Rr	68	69	6A	6B	6C	6D	6E	6F
ADDC A, Rr	78	79	7A	7B	7C	7D	7E	7F
ANL A, Rr	58	59	5A	5B	5C	5D	5E	5F
DEC Rr	C8	C9	CA	CB	CC	CD	CE	CF
DJNZ Rr, addr	E8	E9	EA	EB	EC	ED	EE	EF
INC Rr	18	19	1A	1B	1C	1D	1E	1F
MOV A, Rr	F8	F9	FA	FB	FC	FD	FE	FF
MOV Rr, A	A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr, #data	B8	B9	BA	BB	BC	BD	BE	BF
ORL A, Rr	48	49	4A	4B	4C	4D	4E	4F
XCH A, Rr	28	29	2A	2B	2C	2D	2E	2F
XRL A, Rr	D8	D9	DA	DB	DC	DD	DE	DF

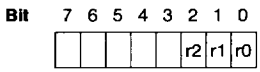


Table 4. OP Codes for Expander Port Access

Mnemonic / Rr	P4	P5	P6	P7
ANLD Pp, A	9C	9D	9E	9F
MOVD A, Pp	0C	0D	0E	0F
MOVD Pp, A	3C	3D	3E	3F
ORLD Pp, A	8C	8D	8E	8F

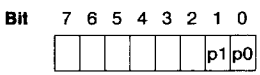
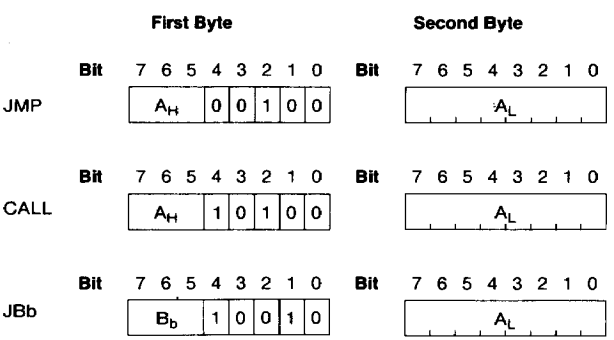


Table 5. OP Codes for JMP, CALL, and JBb



A_H = Address A_{10}, A_9, A_8 **A_L** = Address A_7 to A_0 **Bb** = b^{th} bit of accumulator

INSTRUCTION CODES

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP		OUT DBB,A	ADD A, #	JMP 0 x x	EN I		DEC A		IN A, P1	IN A, P2		MOVD A, P4	MOVD A, P5	MOVD A, P6	MOVD A, P7
1	INC @R0	INC @R1	JB0 addr	ADDC A, #	CALL 0 x x	DIS I	JTF addr	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
2	XCH A, @R0	XCH A, @R1	IN A, DBB	MOV A, #	JMP 1 x x	EN TCNTI	JNT0 addr	CLR A	XCH A, R0	XCH A, R1	XCH A, R2	XCH A, R3	XCH A, R4	XCH A, R5	XCH A, R6	XCH A, R7
3	XCHD A, @R0	XCHD A, @R1	JB1 addr		CALL 1 x x	DIS TCNTI	JT0 addr	CPL A		OUTL P1, A	OUTL P2, A		MOVD P4, A	MOVD P5, A	MOVD P6, A	MOVD P7, A
4	ORL A, @R0	ORL A, @R1	MOV A, T	ORL A, #	JMP 2 x x	STRT CNT	JNT1 addr	SWAP A	ORL A, R0	ORL A, R1	ORL A, R2	ORL A, R3	ORL A, R4	ORL A, R5	ORL A, R6	ORL A, R7
5	ANL A, @R0	ANL A, @R1	JB2 addr	ANL A, #	CALL 2 x x	STRT T	JT1 addr	DA A	ANL A, R0	ANL A, R1	ANL A, R2	ANL A, R3	ANL A, R4	ANL A, R5	ANL A, R6	ANL A, R7
6	ADD A, @R0	ADD A, @R1	MOV T, A		JMP 3 x x	STOP TCNT		RRC A	ADD A, R0	ADD A, R1	ADD A, R2	ADD A, R3	ADD A, R4	ADD A, R5	ADD A, R6	ADD A, R7
7	ADDC A, @R0	ADDC A, @R1	JB3 addr		CALL 3 x x		JF1 addr	RR A	ADDC A, R0	ADDC A, R1	ADDC A, R2	ADDC A, R3	ADDC A, R4	ADDC A, R5	ADDC A, R6	ADDC A, R7
8				RET	JMP 4 x x	CLR F0	JOBF addr			ORL P1, #	ORL P2, #		ORLD P4, A	ORLD P5, A	ORLD P6, A	ORLD P7, A
9	MOV STS, A		JB4 addr	RETR	CALL 4 x x	CPL F0	JNZ addr	CLR C		ANL P1, #	ANL P2, #		ANLD P4, A	ANLD P5, A	ANLD P6, A	ANLD P7, A
A	MOV @R0, A	MOV @R1, A		MOVP A, @A	JMP 5 x x	CLR F1		CPL C	MOV R0, A	MOV R1, A	MOV R2, A	MOV R3, A	MOV R4, A	MOV R5, A	MOV R6, A	MOV R7, A
B	MOV @R0, #	MOV @R1, #	JB5 addr	JMPP @A	CALL 5 x x	CPL F1	JF0 addr		MOV R0, #	MOV R1, #	MOV R2, #	MOV R3, #	MOV R4, #	MOV R5, #	MOV R6, #	MOV R7, #
C					JMP 6 x x	SEL RB0	JZ addr	MOV A, PSW	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
D	XRL A, @R0	XRL A, @R1	JB6 addr	XRL A, #	CALL 6 x x	SEL RB1	JNIBF addr	MOV PSW, A	XRL A, R0	XRL A, R1	XRL A, R2	XRL A, R3	XRL A, R4	XRL A, R5	XRL A, R6	XRL A, R7
E				MOVP3 A,@A	JMP 7 x x	EN DMA	JNC addr	RL A	DJNZ R0, addr	DJNZ R1, addr	DJNZ R2, addr	DJNZ R3, addr	DJNZ R4, addr	DJNZ R5, addr	DJNZ R6, addr	DJNZ R7, addr
F	MOV A, @R0	MOV A, @R1	JB7 addr		CALL 7 x x	EN FLAGS	JC addr	RLC A	MOV A, R0	MOV A, R1	MOV A, R2	MOV A, R3	MOV A, R4	MOV A, R5	MOV A, R6	MOV A, R7

Legend:

\# = Immediate data

= 1 Byte, 1 Cycle Instruction

= 1 Byte, 2 Cycle Instruction

= 2 Byte, 2 Cycle Instruction

4

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Ambient Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.5	W

Note:
Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}, V_{DD}	4.5	5.0	5.5	V
	V_{SS}		0		V
Operating Temperature	T_A	0		+70	°C

DC Characteristics

T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ± 10%, V_{SS} = 0V

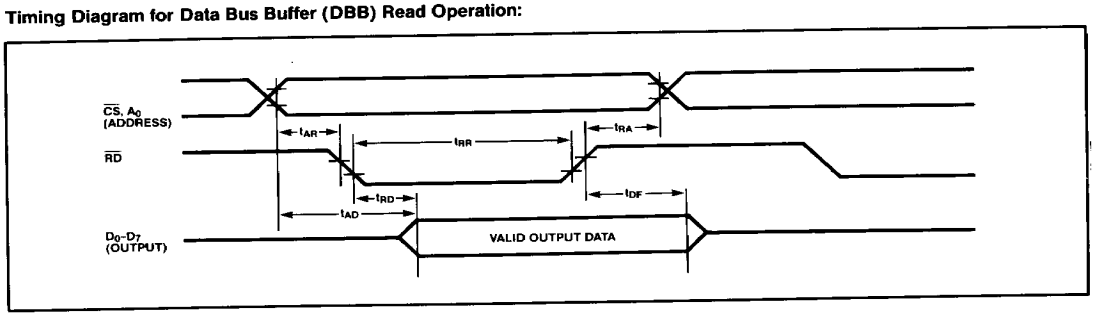
Parameter		Symbol	Test Conditions	Value		Unit
				Min	Max	
V_{DD} Supply Current		I_{DD}			20	mA
Supply Current		I_{CC} + I_{DD}			150	mA
Input Low Voltage	All except XTAL1, 2, $\overline{RESET}$	V_{IL}		-0.3	0.8	V
	XTAL1, 2, $\overline{RESET}$	V_{IL1}		-0.3	0.6	V
Input High Voltage	All except XTAL1, 2, $\overline{RESET}$	V_{IH}		2.0	V_{CC}	V
	XTAL1, 2, $\overline{RESET}$	V_{IH1}		3.8	V_{CC}	V
Output Low Voltage	D_0 to D_7	V_{OL}	I_{OL} = 2.0mA		0.45	V
	P10 to P17, P20 to P27, SYNC	V_{OL1}	I_{OL} = 1.6mA		0.45	V
	PROG	V_{OL2}	I_{OL} = 1.0mA		0.45	V
Output High Voltage	D_0 to D_7	V_{OH}	I_{OH} = -400μA	2.4		V
	All other outputs	V_{OH1}	I_{OH} = -50μA	2.4		V
Input Leakage Current	T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0, EA	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$		±10	μA
Output Leakage Current	D_0 to D_7 (High-impedance)	I_{OL}	V_{SS} + 0.45V ≤ $V_{IN} \leq V_{CC}$		±10	μA
Input Low Current	P10 to P17; P20 to P27	I_{LI}	V_{IL} = 0.8V		0.5	mA
	$\overline{RESET}$, $\overline{SS}$	I_{LI1}	V_{IL} = 0.8V		0.2	mA

AC Characteristics (DBB Read Operation)

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V)

Parameter		Symbol	Test Conditions	Value		Unit
				Min	Max	
$\overline{CS}$, A0 Setup Time (to $\overline{RD}$ ↓)		t_{AR}		0		ns
$\overline{CS}$, A0 Hold Time (to $\overline{RD}$ ↑)		t_{RA}		0		ns
$\overline{RD}$ Pulse Width		t_{RR}		160		ns
Data Delay Time (from $\overline{CS}$, A0)		t_{AD}	C_L = 150pF		130	ns
Data Delay Time (from $\overline{RD}$ ↓)		t_{RD}	C_L = 150pF		130	ns
Data Floating Time (from $\overline{RD}$ ↑)		t_{DF}			85	ns
Cycle Time	MBL8742N	t_{CY}	6MHz (N-version)	2.5	15.0	μs
	MBL8742H		12MHz (H-version)	1.25	15.0	μs

Timing Diagram for Data Bus Buffer (DBB) Read Operation:



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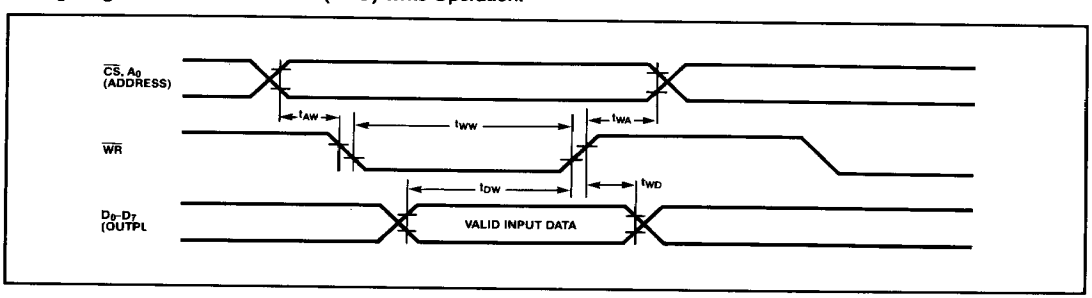
AC Characteristics (DBB Write Operation)

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	Value		Unit
			Min	Max	
$\overline{CS}$, A0 Setup Time (to $\overline{WR}$ ↓)	t_{AW}		0		ns
$\overline{CS}$, A0 Hold Time (from $\overline{WR}$ ↑)	t_{WA}		0		ns
$\overline{WR}$ Pulse Width	t_{WW}		160		ns
Data Setup Time (to $\overline{WR}$ ↑)	t_{DW}		130		ns
Data Hold Time (from $\overline{WR}$ ↑)	t_{WD}		0		ns

Timing Diagram for Data Bus Buffer (DBB) Write Operation:

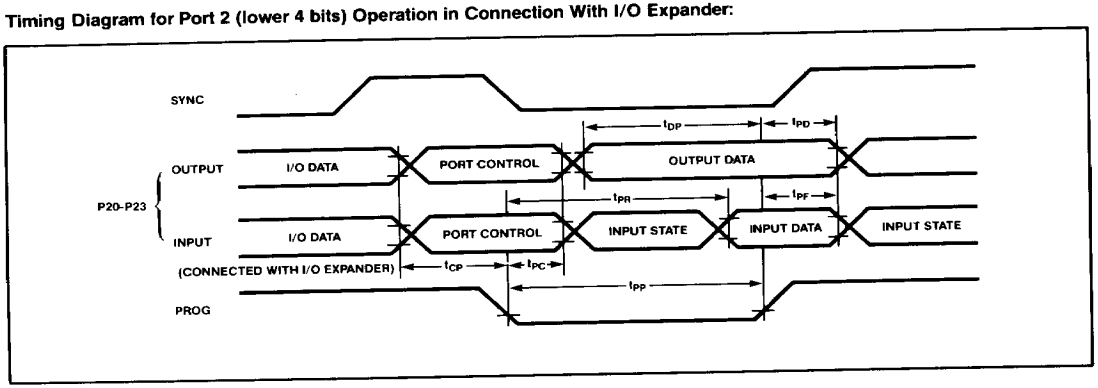


AC Characteristics (Operation with I/O Expander)

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V)

Parameter	Symbol	MBL8742N		MBL8742H		Unit
		Min	Max	Min	Max	
Port Control Setup Time (to PROG ↓)	t_{CP}	100		110		ns
Port Control Hold Time (from PROG ↓)	t_{PC}	60		100		ns
Input Data Delay Time (from PROG ↓)	t_{PR}		650		810	ns
Input Data Hold Time (from PROG ↑)	t_{PF}	0	150	0	150	ns
Output Data Setup Time (to PROG ↑)	t_{DP}	200		250		ns
Output Data Hold Time (from PROG ↑)	t_{PD}	20		65		ns
PROG Pulse Width	t_{PP}	700		1200		ns

Timing Diagram for Port 2 (lower 4 bits) Operation in Connection With I/O Expander:



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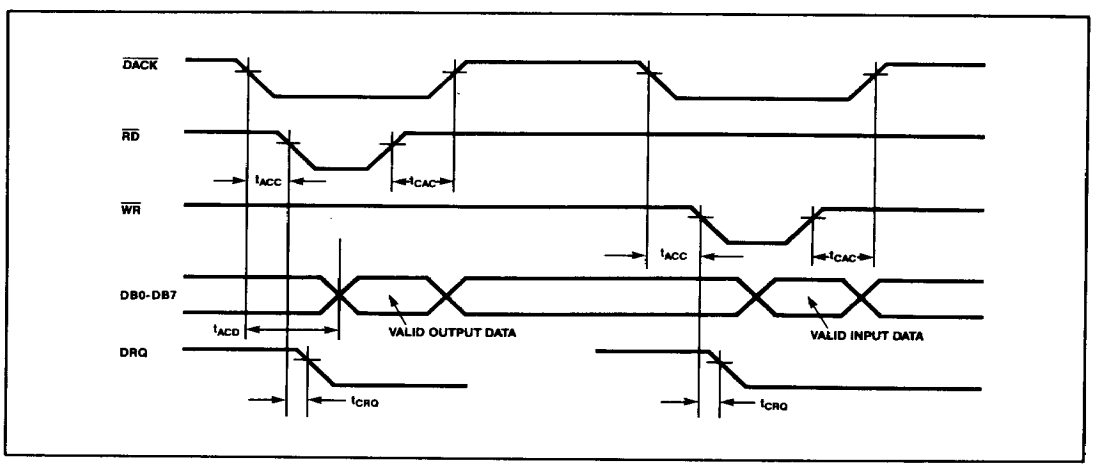
AC Characteristics (DMA Operation)

(T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5.0V ±10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	Value		Unit
			Min	Max	
$\overline{DACK}$ Setup Time (to $\overline{RD}$ ↓, $\overline{WR}$ ↓)	t_{ACC}		0		ns
$\overline{DACK}$ Hold Time (from $\overline{RD}$ ↑, $\overline{WR}$ ↑)	t_{CAC}		0		ns
Input Data Delay Time (from $\overline{DACK}$ ↓)	t_{ACD}	C_L = 150pF		130	ns
DRQ Clear Time (from $\overline{RD}$ ↓, $\overline{WR}$ ↓)	t_{CRQ}			100	ns

Timing Diagram for DMA Operation:



TEST CONDITIONS

V_{IL} = 0.8V (All except XTAL1, 2, $\overline{RESET}$)
= 0.6V (XTAL1, 2, $\overline{RESET}$)

V_{IH} = 2.0V (All except XTAL1, 2, $\overline{RESET}$)
= 3.8V (XTAL1, 2, $\overline{RESET}$)

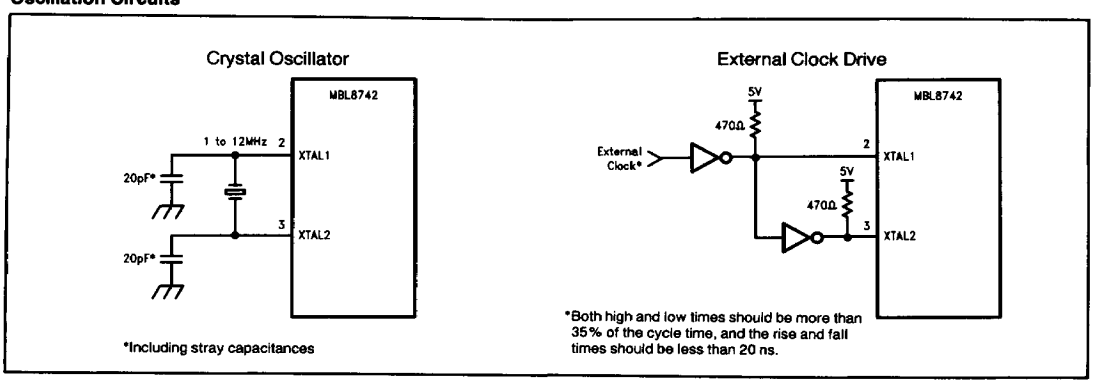
V_{OL} = 0.45V

V_{OH} = 2.4V

OUTPUT LOAD

D0 to D7: C_L = 150pF
All other outputs: C_L = 80pF

Oscillation Circuits



ELECTRICAL CHARACTERISTICS FOR PROGRAMMING

DC Characteristics[1,2]

(T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 21 ±0.5V or 5V ±5%)

Parameter	Symbol	Value		Unit
		Min	Max	
V_{DD} Program Voltage High Level	V_{DDH}	20.5	21.5	V
V_{DD} Program Voltage Low Level	V_{DDL}	4.75	5.25	
PROG Program Voltage High Level	V_{PH}	17.5	18.5	V
PROG Program Voltage Low Level	V_{PL}	—	0.2	
EA Program/Verify Voltage High Level	V_{EAH}	17.5	18.5	V
EA Program/Verify Voltage Low Level	V_{EAL}	—	5.25	
V_{DD} High Voltage Supply Current	I_{DD}	—	30.0	mA
PROG High Voltage Supply Current	I_{PROG}	—	16.0	
EA High Voltage Supply Current	I_{EA}	—	1.0	

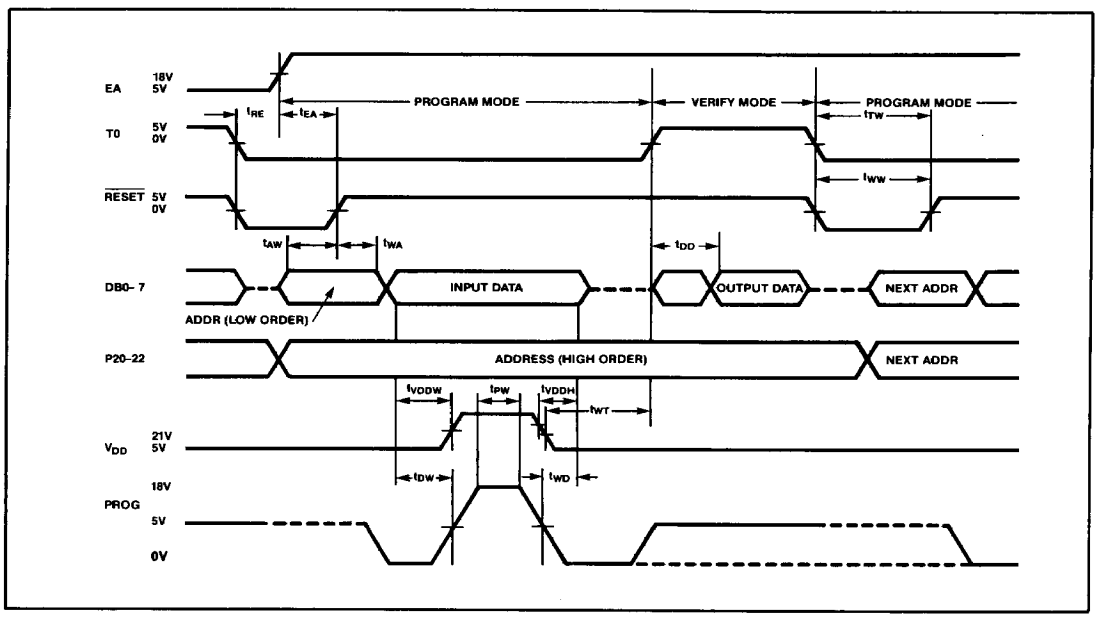
Notes:
1. High Level Voltage (V_{DDH}, V_{PH}) should not be applied to V_{DD} and PROG pins unless V_{CC} = 5V ±5% and EA = 18V ±0.5V.
2. V_{DD}, PROG, and EA should not exceed the above specified range, including overshoot and undershoot.

AC Characteristics

(T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 21 ±1.0V or 5V ±5%)

Parameter	Symbol	Value		Unit
		Min	Max	
Address setup time (before $\overline{\text{RESET}}$ ↑)	t_{AW}	$4 \cdot t_{CY}$	—	
Address hold time (after $\overline{\text{RESET}}$ ↑)	t_{WA}	$4 \cdot t_{CY}$	—	
Input data setup time (before $\overline{\text{PROG}}$ ↑)	t_{DW}	$4 \cdot t_{CY}$	—	
Input data hold time (after $\overline{\text{PROG}}$ ↓)	t_{WD}	$4 \cdot t_{CY}$	—	
$\overline{\text{RESET}}$ hold time (after EA ↓)	t_{PH}	$4 \cdot t_{CY}$	—	
V_{DD} setup time (before PROG ↑)	t_{VDDW}	$4 \cdot t_{CY}$	—	
V_{DD} hold time (before PROG ↓)	t_{VDDH}	0	—	
Program pulse width	t_{PW}	50	60	ms
TO setup time (before RESET ↑)	t_{TW}	$4 \cdot t_{CY}$	—	
TO hold time (after V_{DD} ↓)	t_{WT}	$4 \cdot t_{CY}$	—	
Data output delay time (after TO ↑)	t_{DO}	—	$4 \cdot t_{CY}$	
RESET pulse width (to Latch Address)	t_{WW}	$4 \cdot t_{CY}$	—	
V_{DD} and PROG rise/fall time	tr/tf	0.5	2.0	μs
MPU cycle time	t_{CY}	5.0	—	μs
$\overline{\text{RESET}}$ setup time (before EA ↑)	t_{RE}	$4 \cdot t_{CY}$	—	
EA setup time (before $\overline{\text{RESET}}$ ↑)	t_{EA}	10	—	ms

Timing Diagram for Programming/Verify Mode:



PACKAGE DIMENSIONS

40-Lead Ceramic (Metal Seal)
Dual In-Line Package
(Case No.: DIP-40C-A04)